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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EDWARD COLLES NEVILL

Appeal 2009-014323
Application 10/066,475[1]
Technology Center 2400

Decided: March 8, 2010

Before ROBERT E. NAPPI, JOHN A. JEFFERY, and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-70. We have jurisdiction under 35 U.S.C. § 6(b), and we heard the appeal on March 3, 2010. We affirm-in-part.

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[1] This application seeks to reissue U.S. Patent 6,021,265.

STATEMENT OF THE CASE

Appellant invented a data processing system that switches between multiple instruction sets (e.g., 16-bit and 32-bit instruction sets). This switching is effected by writing a target address and a "mode flag" (T) to a program counter register as part of the execution of a branch instruction. *See generally* Abstract; Spec. col. 4, ll. 6-60; col. 6, ll. 23-53; Fig. 1.[2] Claims 1 and 65 are illustrative with key disputed limitations emphasized:

1. Data processing apparatus comprising:

(i) a processor core operable to execute successive program instruction words of a predetermined plurality of instruction sets stored in a data memory;

(ii) a program counter register for indicating an address of a next program instruction word in said data memory;

(iii) logic operable to modify the contents of said program counter register in response to a current program instruction word;

(iv) a processor core controller, responsive to one or more predetermined indicator bits of said program counter register, operable to control said processor core to execute program instruction words of a current instruction set selected from said predetermined plurality of instruction sets and specified by the state of said one or more indicator bits of said program counter register; and

(v) a memory access controller operable to access program instruction words stored in said data memory, said *access controller not being responsive to said one or more indicator bits of said program counter register.*

[2] This citation is to the original patent (US 6,021,265).

65. A program counter register comprising:

an ordered set of bits:

wherein a subset of the ordered set of bits identifies an address of an instruction; and at least one bit of the ordered set of bits identifies an instruction set; and

wherein *the at least one bit is not a member of the subset.*

The Examiner relies on the following as evidence of unpatentability:

Larsen	US 5,115,500	May 19, 1992

THE REJECTION

The Examiner rejected claims 1-70 under 35 U.S.C. § 102(b) as anticipated by Larsen. Ans. 3-15.[3]

CLAIM GROUPING

Appellant argues the following claim groupings separately: (1) claims 1-14; (2) claims 15-20 and 51-56; (3) claims 21-26, 33-38, 45-50, and 57-64; (4) claims 27-32 and 39-44; (5) claim 65; and (6) claims 66-70. *See* App. Br. 16-23. Accordingly, we select claims 1, 15, 21, 27, and 66 as representative of groups (1)-(4) and (6), respectively. *See* 37 C.F.R. § 41.37(c)(1)(vii).

[3] Throughout this opinion, we refer to (1) the Appeal Brief filed November 27, 2006; (2) the Examiner's Answer mailed May 19, 2008; and (3) the Reply Brief filed July 11, 2008.

CONTENTIONS

Regarding independent claim 65, the Examiner finds that Larsen discloses an "ordered set" of bits (i.e., all bits from Larsen's instruction address register (IAR) 3). According to the Examiner, since the top three bits of this ordered set identify the instruction set via the instruction decode selection register (IDSR) 10, these top three bits are therefore not part of the "subset" of the remaining bits that identify an instruction address (i.e., the bits other than the top three bits). Ans. 3, 4, 15, 16.

Appellant argues that there cannot be a subset of bits in Larsen that specifies the instruction address since the address is the entire sequence of bits from the IAR. According to Appellant, since Larsen uses *all* bits to specify instruction addresses, and *reuses* the top three bits of this address to specify an instruction set, then there is no bit used to identify the instruction set that is not used to specify an instruction address as claimed. App. Br. 22-23; Reply Br. 4-9, 11, 12; emphases added.

Regarding representative claim 1, Appellant contends that Larsen fails to anticipate the claim since any part of Larsen's system responsible for controlling access to I-store 2 must be responsive to bits used to specify the instruction set (i.e., the three highest-order bits of the IAR). App. Br. 16-20; Reply Br. 10. The Examiner contends that the claim does not preclude the top three bits from the IAR from specifying both the instruction address and the instruction set. Ans. 17.

Regarding representative claim 15, Appellant argues that since Larsen's address always specifies the instruction set, the instruction set cannot be identified by the bit sequence's instruction set indicator portion

without regard to the derived address from the sequence's address portion as claimed. App. Br. 20; Reply Br. 10.

Appellant makes similar arguments regarding representative claim 21 and contends that Larsen fails to disclose that bit sequence's instruction set indicator portion has a bit that is not part of the sequence's address portion. App. Br. 20-21; Reply Br. 11. Appellant makes similar arguments regarding representative claims 27 and 66 regarding Larsen's alleged failure to set a control flag specifying the instruction set without regard to the derived address from the sequence's address portion. App. Br. 21-23; Reply Br 11-12.

The issues before us, then, are as follows:

ISSUES

Under § 102, has the Examiner erred by finding that Larsen discloses:

(1) an ordered set of bits where a subset of these bits identifies an instruction address, and at least one bit of the ordered set that is not a member of the subset identifies an instruction set as recited in claim 65?

(2) a memory access controller that is not responsive to one or more indicator bits of the program counter register as recited in claim 1?

(3) identifying an instruction set by an instruction set indicator portion of a bit sequence without regard to the address derived from the sequence's address portion as recited in claim 15?

(4) accessing a sequence of bits with an address portion and an instruction set indicator portion, where the instruction set indicator portion has at least one bit that is not part of the address portion as recited in claim 21?

(5) setting a control flag without regard to the address derived from the address portion of the bit sequence as recited in claim 27?

(6) setting the value of a flag that is not dependent upon the next instruction's address as recited in claim 66?

FINDINGS OF FACT

1. Larsen's system decodes and executes plural incompatible instructions (e.g., with different formats). These instructions are placed in predefined areas of an instruction store ("I-store") 2, and are decoded based on (1) where in the I-store the fetched instruction resided, and (2) the instruction itself. Larsen, Abstract; col. 1, ll. 1-10; col. 3, ll. 52-57; Figs. 1A and 2.

2. Instructions fetched from I-store 2 are placed into instruction decode register (IDR) 1. The IDR is connected to instruction decode memory (IDM) 5. Larsen, col. 3, ll. 53-58; Fig. 2.

3. IAR 3 contains the I-store address for the fetched instruction, and is connected to the I-store and IDSR 10. The IDSR (1) contains only the three high-order bits from the IAR, and (2) is connected to the IDM. Larsen, col. 5, ll. 53-58; Fig. 2.

4. The I-store is partitioned in eight equal partitions such that the three high-order address bits not only define which partition is addressed, but also the type of instruction associated with that address. To this end, the I-store's high-order addresses (i.e., beginning with "111") are reserved for "Type 2" instructions, and the remaining addresses are reserved for "Type 1" instructions. Larsen, col. 5, ll. 41-51; col. 5, l. 64 – col. 6, l. 2; Fig. 2.

5. The contents of the IDSR 10 and IDR 1 are taken together to provide a look-up address within IDM 5. Decoding of instructions in IDR 1 therefore depends not only on the contents of IDR 1, but also on the region of the I-store from which the instruction was fetched (i.e., the portion of the address provided by the IDSR). Larsen, col. 6, ll. 3-16; Fig. 2.

ANALYSIS

Claim 65

Based on the record before us, we find no error in the Examiner's anticipation rejection of claim 65. This claim calls for a register with an ordered set of bits where a subset of these bits identifies an instruction address, and at least one bit of the ordered set that is not a member of the subset identifies an instruction set.

We note at the outset that merely reciting a register's bits and specifying what these bits identify essentially constitutes non-functional descriptive material as it merely specifies the register's informational content, and therefore does not further limit the claimed invention either functionally or structurally. Such non-functional descriptive material does not patentably distinguish over prior art that otherwise renders the claims unpatentable.[4]

Nevertheless, even if the respective identifications associated with various bits within the "ordered set" did limit claim 65 (which they do not), we find no error in the Examiner's position based on Larsen given the

[4] *See In re Ngai*, 367 F.3d 1336, 1339 (Fed. Cir. 2004); *see also Ex parte Nehls*, *see also Ex parte Nehls*, 88 USPQ2d 1883, 1887-89 (precedential) (discussing cases pertaining to non-functional descriptive material).

claim's scope and breadth. Notably, the claim merely recites, in pertinent part, that "a subset of the ordered set of bits identifies *an* address of *an* instruction" (emphases added). Nothing in the claim requires that this address be *complete*—or even *correct*—let alone that it corresponds to the same instruction set identified by other bit(s) of the ordered set as claimed. Rather, this limitation is fully met so long as a subset of the ordered set of bits identifies *an* address of *an* instruction—even partial or incorrect addresses.

Turning to Larsen, the Examiner equates all address bits from Larsen's IAR with the recited "ordered set" of bits. Although the Examiner acknowledges that the top three bits of this "ordered set" identify the instruction set via the IDSR 10, these top three bits are nonetheless not part of the "subset" of the *remaining* bits that identify an instruction address (i.e., the bits other than the top three bits). Ans. 3, 4, 15, 16.

Despite Appellant's contentions to the contrary, we see no error in this interpretation given the scope of the claim. That said, Appellant is correct (Reply Br. 4-9) that the top three bits of the instruction address from Larsen's IAR also indicate the type of instruction (i.e., "Type 1" or "Type 2"). FF 3-4. Nevertheless, the remaining low-order address bits (i.e., the "subset" of bits distinct from the top three bits) would identify at least a partial address of an instruction—a fact that Appellant readily acknowledges. *See* Reply Br. 8 (acknowledging that the remaining five bits of Larsen's instruction address "only provide *part of an address* and are ambiguous at best") (emphasis added). Notably, these partial addresses

would be unique to a particular I-store partition depending on the state of the top three bits. *See* FF 4 (noting that the top three address bits identify a particular I-store partition corresponding to the instruction type).

In short, nothing in the claim precludes the Examiner's reliance on the low-order address bits from Larsen's IAR as corresponding to the recited "subset" since these low-order address bits: (1) identify *an* address of *an* instruction (within a given partition selected by the three high-order bits), and (2) are distinct from the three high-order address bits that also identify an instruction set by type (i.e., Type 1 or Type 2). *See* FF 3-4. We reach this conclusion even assuming that Larsen would fail to operate correctly if the top three bits were not used to specify both the instruction's address and its type (*see* FF 5) as Appellant argues (Reply Br. 5-8). Although the top three high-order address bits along with the remaining low-order address bits identify a *complete* address (*see* FF 3-4), this does not negate the Examiner's finding of anticipation which is based on Larsen's identifying at least a *partial* address via the remaining address bits. We find a partial low-order address is "an address" within the broad scope of Appellant's claim 65.

We are therefore not persuaded that the Examiner erred in rejecting claim 65.

Claims 1-14

We will not, however, sustain the Examiner's rejection of independent claim 1 which calls for, in pertinent part, a memory access controller that is *not* responsive to one or more indicator bits of the program counter register.

First, the Examiner is not clear as to which element(s) in Larsen correspond to the recited "memory access controller," let alone explain how

these elements function as such a controller. Although the Examiner generally refers to Larsen's IAR 3, IDSR 10, and I-store 2 in connection with this limitation (Ans. 9), elements 3 and 10 are mapped to other limitations in the claim, namely the program counter register and processor core controller.[5]

Despite these ambiguities, we do not see how any element in Larsen that would constitute a "memory access controller" under its broadest reasonable interpretation[6] would not be responsive to one or more indicator bits of the program counter register as claimed. The IAR provides *all* bits to indicate the address of a fetched instruction; the three high-order bits of which indicate the particular partition corresponding to the instruction (i.e., indicating its type). FF 3-4. Although the low-order address bits from the IAR would indicate a partial address as noted previously, the Examiner has simply failed to show how the specific recited functionality of the memory access controller would not be responsive to the recited indicator bits.

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[5] Although Appellant's characterization that the recited "memory access controller" corresponds to Larsen's address resolving logic 6 (App. Br. 18) is equally puzzling, Appellant nonetheless conceded at the oral hearing that this characterization was incorrect.

[6] Although this limitation was construed by a district court in connection with litigation involving the original patent of this reissue application (US 6,021,265) and the patent corresponding to its parent application (US 5,758,115) (Rel. Proc. App'x), we nevertheless use a different claim construction standard than that used by the court. *See In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (2004). While the court's construction may inform our understanding of the recited limitations, we nonetheless construe the claims giving the terms their broadest reasonable interpretation in light of the Specification. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citations omitted).

We are therefore persuaded that the Examiner erred in rejecting independent claim 1, and dependent claims 2-14 for similar reasons.

Claims 15-20 and 51-56

We will, however, sustain the Examiner's rejection of representative claim 15. As we indicated previously, the three high-order bits from Larsen's IAR indicate a type of instruction (FF 3-4) and therefore constitute an "instruction set indicator portion" of the bit sequence from the IAR. Likewise, the remaining low-order bits constitute an "address portion" of that sequence since these bits indicate at least a partial address as noted previously. The instruction set or type of instruction (i.e., whether it is "Type 1" or "Type 2") can therefore be identified by the first three bits of this sequence, and without regard to at least the partial address derived from the remaining low-order bits. *See id.* The limitation is therefore fully met by Larsen.

We are therefore not persuaded that the Examiner erred in rejecting representative claim 15, and claims 16-20 and 51-56 which fall with claim 15.

Claims 21-26, 33-38, 45-50, and 57-64

We will also sustain the Examiner's rejection of representative claim 21 for the reasons indicated previously. In short, nothing in the claim precludes the "address portion" of the bit sequence from corresponding to the at least partial address indicated by the low-order address bits of

Larsen's IAR. *See* FF 3-4. Larsen's "instruction set indicator portion" (top three bits from the IAR) would therefore not be part of the low-order "address portion."

We are therefore not persuaded that the Examiner erred in rejecting representative claim 21, and claims 22-26, 33-38, 45-50, and 57-64 which fall with claim 21.

Claims 27-32, 39-44, and 66-70

We will also sustain the Examiner's rejection of representative claim 27 for the reasons indicated previously. Nor has Appellant shown error in the Examiner's finding regarding Larsen's setting control flags associated with the instruction set (Ans. 14-15). We are therefore not persuaded that the Examiner erred in rejecting representative claim 27, and claims 28-32 and 39-44 which fall with claim 27. We reach a similar conclusion regarding representative claim 66 (calling for setting the value of a flag not dependent upon the instruction address), and claims 67-70 which fall with claim 66.

CONCLUSION

The Examiner did not err in rejecting claims 15-70 under § 102, but erred in rejecting claims 1-14 under § 102.

ORDER

The Examiner's decision rejecting claims 1-70 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

pgc

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